

Savitch's Theorem Theorem: STCONN ⊆ SPACE(log² n) • Corollary: NL ⊆ SPACE(log²n) • Corollary: NPSPACE = PSPACE

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/* return true iff path from x to y of length at most 2ⁱ */ PATH(x, y, i) if i = 0 return (x = y or (x, y) $\in E$) for z in V if PATH(x, z, i-1) and PATH(z, y, i-1) return(true); return(false);

end

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- recursive algorithm:

Proof of Theorem

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/* base case */

- input: G = (V, E), two nodes s and t

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Proof of Theorem

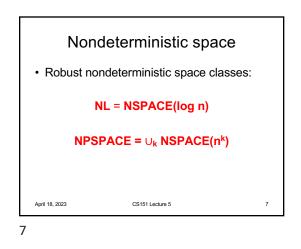
- answer to STCONN: PATH(s, t, log n)
- space used:
 - (depth of recursion) x (size of "stack record")
- depth = log n
- claim stack record: "(x, y, i)" sufficient • size O(log n)
- when return from PATH(a, b, i) can figure out what to do next from record (a, b, i) and previous record

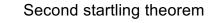
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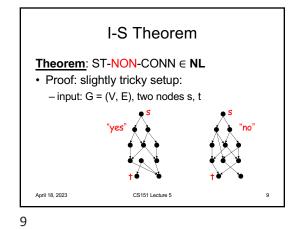


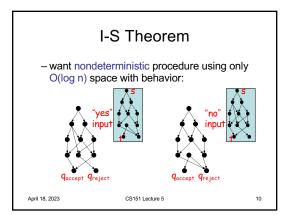


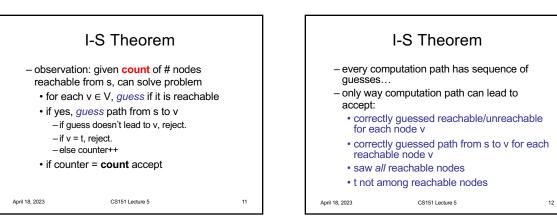
- Strongly believe NP ≠ coNP
- seems impossible to convert existential into universal
- for space: Immerman/Szelepscényi '87/'88:

NL = coNL







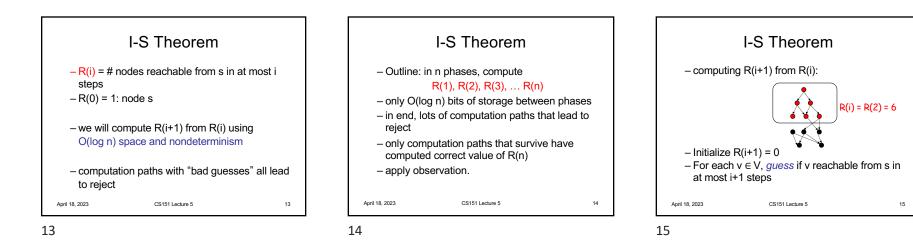


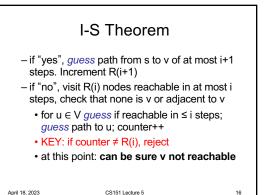
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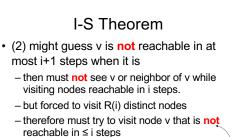




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I-S Theorem • correctness of procedure: two types of errors we can make • (1) might guess v is reachable in at most i+1 steps when it is not - won't be able to guess path from s to v of correct length, so we will reject. "easy" type of error CS151 Lecture 5 17 April 18, 2023



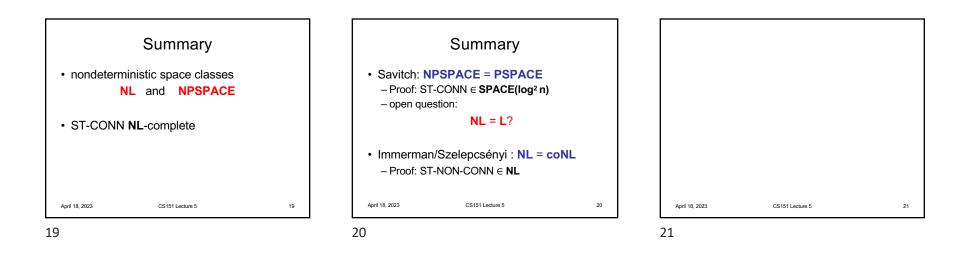
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"easy" type of error

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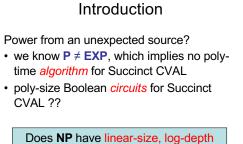
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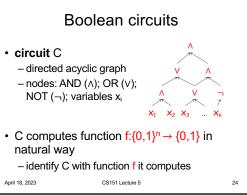
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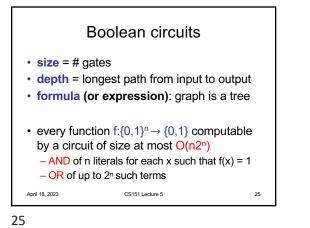


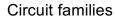
Boolean circuits ?? CS151 Lecture 5 April 18, 2023

Outline Boolean circuits and formulas • circuit C uniformity and advice • the **NC** hierarchy and parallel computation · the quest for circuit lower bounds • a lower bound for formulas natural way CS151 Lecture 5 23 April 18, 2023









- circuit works for specific input length
- we're used to $f: \Sigma^* \rightarrow \{0, 1\}$
- circuit family : a circuit for each input length C₁, C₂, C₃, ... = "{C_n}"
- "{C_n} computes f" iff for all x

 $C_{|x|}(x) = f(x)$

 "{C_n} decides L", where L is the language associated with f

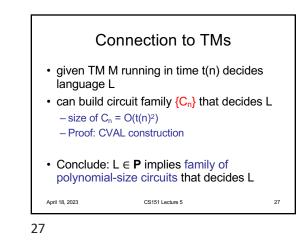
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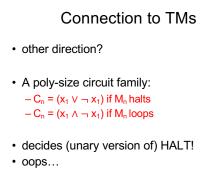
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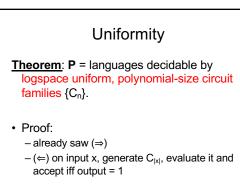


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- Strange aspect of circuit family: – can "encode" (potentially uncomputable) information in family specification
- solution: uniformity require specification is simple to compute
 <u>Definition</u>: circuit family {C_n} is logspace uniform iff TM M outputs C_n on input 1ⁿ and runs in O(log n) space

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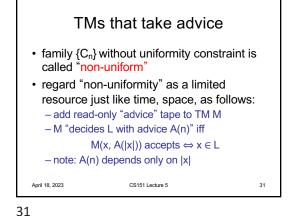


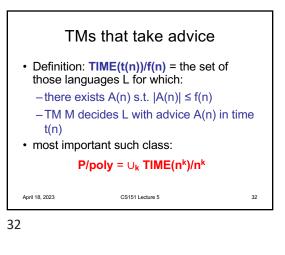
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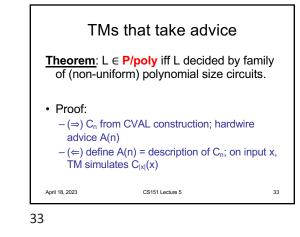
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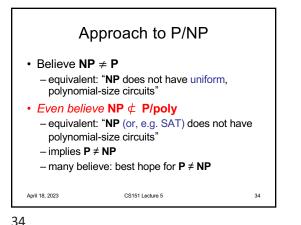
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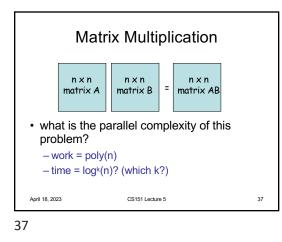


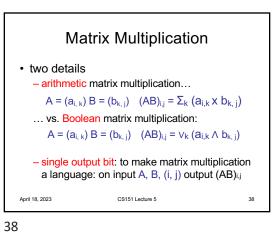


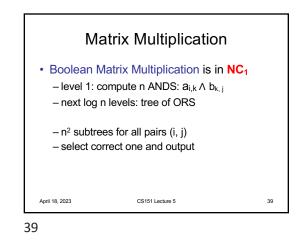


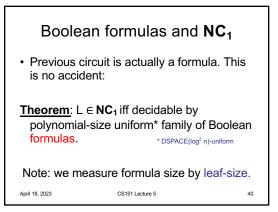


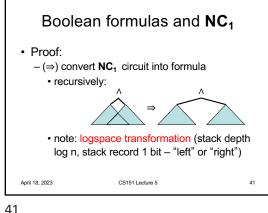
 Parallelism
the NC ("Nick's Class") Hierarchy (of logspace uniform circuits):
NC_k = O(log^k n) depth, poly(n) size NC = U_k NC_k
captures "efficiently parallelizable problems"
not realistic? overly generous
OK for proving non-parallelizable

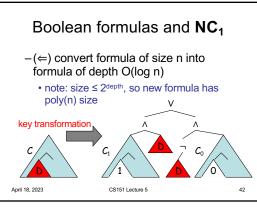


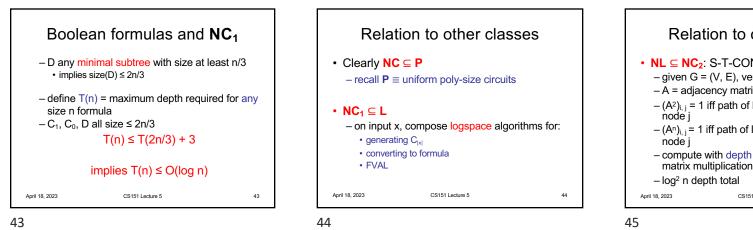


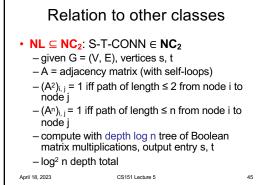


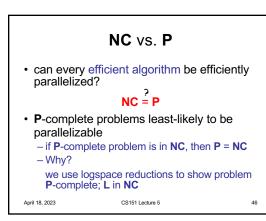












NC vs. P • can every uniform, poly-size Boolean circuit family be converted into a uniform, poly-size Boolean formula family? $NC_1 = P$ April 18, 2023 CS151 Lecture 5 47

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