California Institute of Technology
Department of Computer Science
Computer Architecture

CS184a, Winter 2003 # Assignment 5: Wiring Requirements Monday, February 3

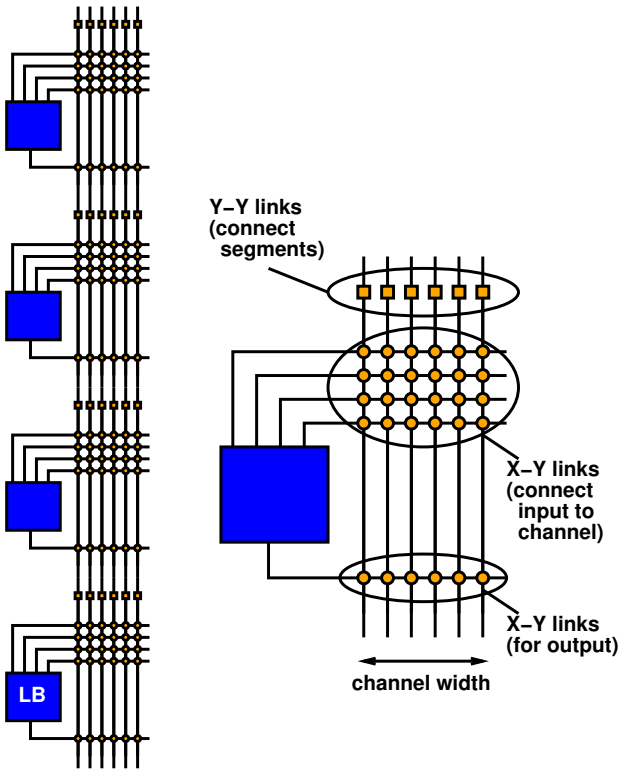
Due: Monday, Februrary 10, 9:00AM

For this assignment, we will compute wiring requirements for your Cascaded 4-LUT pattern match design from the previous assignment.

[If you do not already have a CS account, please get one this week. Next week's assignment will require that you use software on the CS cluster.]

1. Consider using a crossbar for the interconnection of your logic blocks. Assume your primitive substrate has exactly the right number of logic blocks, inputs, and outputs to support your design.
   (a) Identify the size of the crossbar (total inputs x outputs, justify your numbers).
   (b) How many total switches does the crossbar require?

2. Consider a 1D-segmented bus configuration. Again, assume the primitive substrate has exactly the right number of logic blocks to support your design. The external input stream enters on one end of the bus (let's say the top), and your output should exit the opposite end (bottom).



(a) Layout your components in 1D to minimize the number of channels needed. (show your layout and routing in an appropriate, unambiguous manner; it should be possible to easily see the span of each wire segment in your diagram.)

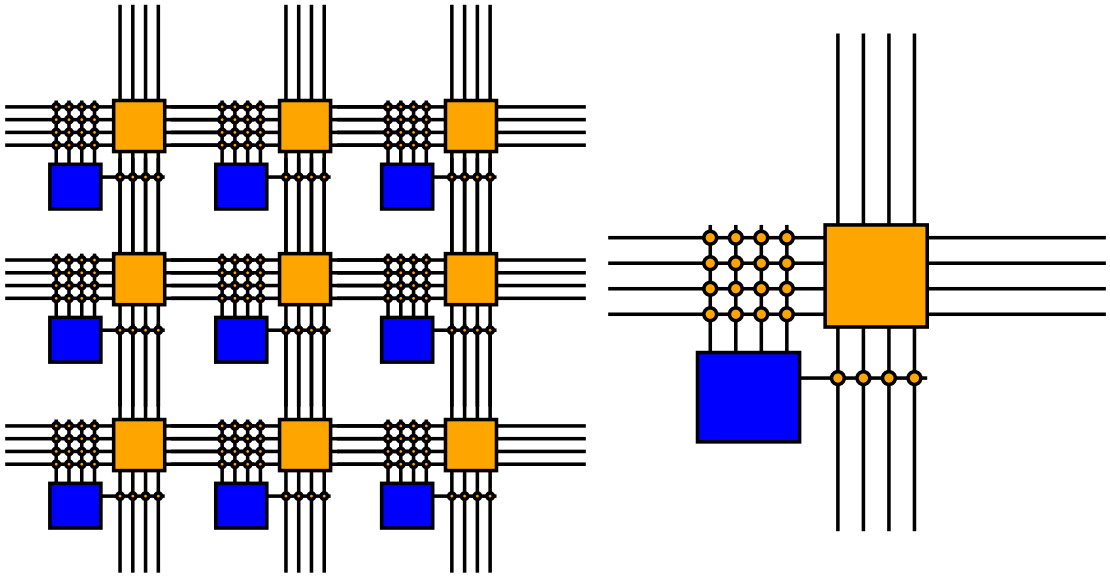
(b) What is the minimum channel width needed to support your design?

(c) How many total switches does this minimum size segmented bus require?

(d) Based on your 1D layout, recursively bisect the design into successively smaller groups of contiguous logic blocks and note the total number of IOs into each of the groups. (*e.g.* If your design took 22 logic blocks, then you would have one cluster of size 22 with the IO from the overall design. You would have two clusters of size 11, then 4 clusters of size 5 or 6 (2 of each), then 8 clusters of size 2 or 3 (2 of size 2, 6 of 3), then you would have another 6 clusters of size 2 (bisecting the 3's), and finally 22 clusters of size 1). Collect the full set of partion size and IO data. Based on this, calculate Rent's rule parameters for your design. (based on the maximum number of IOs for a given partition size? based on the average?)

3. Consider a 2D-array configuration.
   Assume the array is the smallest rectangular region into which your design placement from the previous assignment will fit.

   Assume the switchbox at the intersection of channels provides full connectivity to the adjacent channels. That is, it is made up of 4 $3w \times w$ crossbars; where w is the channel width.



   (a) Route your design to minimize channel width. (I want a nice picture here which clearly shows each routed link.)

   (b) What is the maximum number of routes which share a channel in your routed design? (This is the minimum channel width for which your design is routable.)

   (c) At this minimum channel width, how many switches does your design require?

   (d) Consider depopulating the switchbox so that it only holds $6w$ switches (each wire entering the switchbox may go straight, turn left, or turn right...but only connects to a single channel on each of the three adjacent sides). You are **not** required to reroute your design.

      i. Assuming that the design could still be routed in the channel width identified above, how many switches does the design require?

      ii. How much of a channel expansion could your design experience before the depopulated design required more switches than the fully populated design? (Answer here is a factor. *e.g.* Perhaps my original fit into 4 channels and it would take over 19 channels for the linear population switch count to exceed the full population count. Then I could tolerate a channel expansion factor of 4.75 and still have the linear population scheme require less switches than the full population scheme.)