California Institute of Technology
Department of Computer Science
Computer Architecture

CS184b, Winter 2000   Assignment 1: Architecture   Wednesday, January 3

Due: Tuesday, January 9, 5:00PM

Part A

Work the following problems from Hennessey and Patterson:

- 1.6
- 1.8
- 1.12
- 1.13

Part B

1. At the beginning of the IBM System/360 article, the authors describe the "trends" in computer usage and technology which they felt were key considerations to exploit and which should help define how they architect machines in 1963. 35+ years later, what list would you assemble developing a new architecture? (think, for example, about substrate technology, software technology and techniques, application requirements)

2. Consider a very minimal implementation of some 32b ISA which employed a bit-serial ALU. Assume the bit-serial ALU takes one cycle per bit of datapath processed, so a 32b add instruction would take 32 cycles to complete.

   - how can this support the architectural abstraction?

   - ignoring the 32b ISA, the bit-serial ALU should be efficient (time-space wise, energy wise) computing on small and unusual (non-power-of-two) sized operations. How does the ISA abstraction prevent us from exploiting this feature of this implementation?

   - how would the architectural abstraction need to change to allow us to scale implementations across bit widths, using each bit width efficiently?