**California Institute of Technology**
**Department of Computer Science**
**Computer Architecture**

CS184b, Spring 2003 Assignment 2: Pipelined ISA Monday, April 7

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**Due:** Wednesday, April 16, 9:00AM (but there is no class on Wednesday due to the Student-Faculty Conference)

**Part A:**

1. HP A.1
2. HP A.5

**Part B:**

1. For the `bzip2` you used in the previous assignment, estimate its CPI and hence running time based on the data from `sim-profile`.
   - assume a pipeline structure like the MIPS in Appendix A.
   - assume perfect memory system for now
   - use the aggregate data on instruction, branch, load frequency which you get from `sim-profile` and assume an uniform distribution of instructions, etc.
   - state additional assumptions which you need to make in your calculation
   - show your calculations
2. Run your program under `sim-outorder` in an "inorder" mode and report the running time / CPI.
   - My best guess at a configuration which might come close to modeling a simple, pipelined, scalar processor is given in `/cs/courses/cs184/assign/b2/sim-outorder.invoke`; I've only played with this a little myself, so if you're motivated to look at it more and think there's a better configuration, use it and let me know. I'm hoping the separated, 128K direct-mapped L1 caches backed by a 512K unified L2 cache will give us minimal cache effects here (statistical output from `sim-outorder` will help you verify this assumption or any changes you need to make so it will become true).
   - I have no reason to believe this is that close to what you are calculating above, so don't worry if they're different.
   - We'll be looking at all these ILP and cache issues in weeks ahead, so this exercise is just giving you a chance to use the detailed simulator and develop a base of reference for later experiments where we look at these effects.