

# CS184a: Computer Architecture (Structures and Organization)

Day14: November 10, 2000  
Switching

## Previously

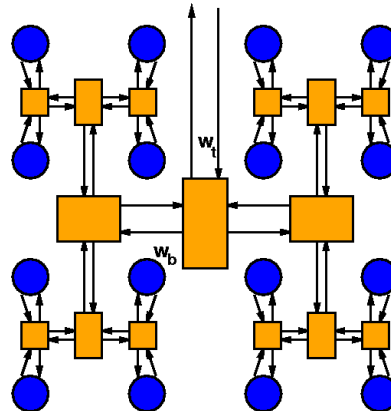
- Role and Requirements for Interconnect
- Understood interconnect structure in terms of recursive bisection
  - *e.g.* Rent's Rule, Hierarchical Interconnect
- Using all necessary wires optimally
  - $O(n^{2p})$  growth
- Raised the question of mesh channel growth
  - $w$  grow as  $n$ ?

# Today

- Switching Requirements
  - use wires
  - reduce switching costs
  - allow routing
- Mesh Interconnect
- Flavor of Switch Timing

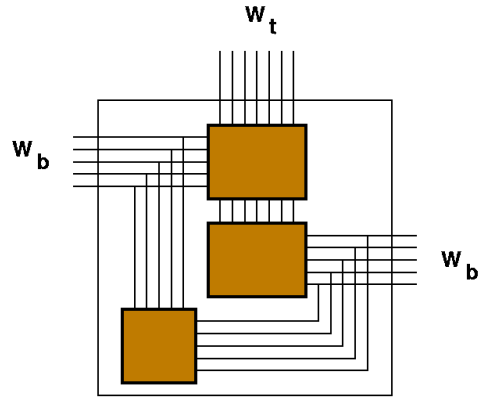
# Hierarchical

- Previously, focussed on wires
- What do switch boxes need to look like to use the wires?



## Straight-forward Case

- Build Crossbars



- Switches:

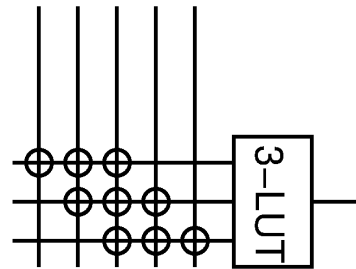
- $w_t \times w_b$
- $w_t \times w_b$
- $w_b \times w_b$
- Total:  $2(w_t \times w_b) + w_b \times w_b$

## Can we do better?

- Crossbar too powerful?
  - Does the specific down channel matter?
- What do we want to do?
  - Connect to *any* channel on lower level
  - Choose a subset of wires from upper level
    - order not important

## N choose K

- Exploit freedom to depopulate switchbox
- Can do with:
  - $K(N-K+1)$  switches



Caltech CS184a Fall2000 -- DeHon

7

## Crossover?

- Specific channel not matter on crossover, either
- But tricky
- Need to guarantee:
  - any subset free on left can be connected to free subset on right
  - can be done in  $w_b^2/2$
  - for large  $w_l/w_b$ , can be done with existing connections

Caltech CS184a Fall2000 -- DeHon

8

## Switching Costs

- How many switches total?
  - What is the switch growth with N?
- How much delay?
  - How does switch delay grow with N?

## Switch Delay

- Switch Delay:  $2 \log_2(N_{\text{tree}})$ 
  - $N_{\text{tree}}$  = smallest subtree containing source and sink
  - Worst Case:  $N_{\text{tree}} = N$

## Switch Area

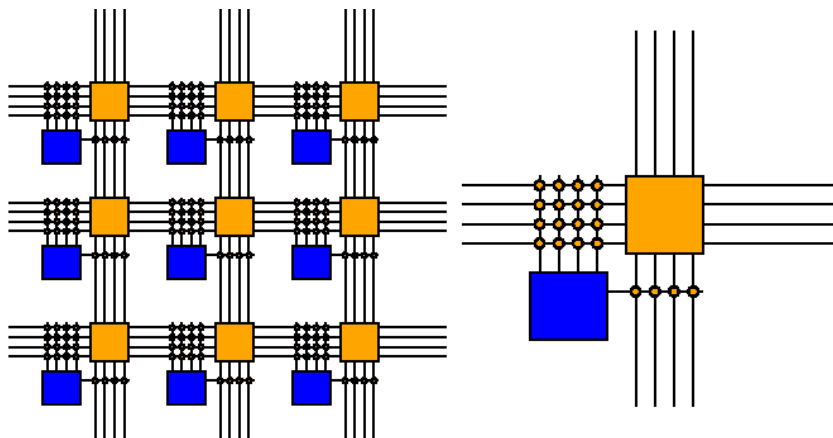
- $w_1 = 2^p w_b$
- $N_{sb}(l) = (2^l - 2^p + 1) w_b^2$
- $N(l) = N / 2^l$
- $w_b(l) = c(2^l)^p$
- $Total = \sum N(l) * N_{sb}(l)$
- $Total \mu \sum (N / 2^l) ((2^l)^p)^2$
- $Total \mu N^{2p} [\sum (1 + 2/2^{2p} + \dots)]$
- $Total \mu N^{2p}$

## Routing

- Trivial and guaranteed
  - assuming don't exceed channel capacities
  - according to the way we just designed the switch boxes
- Start at root switch box:
  - route subset to each side (k of m guarantee)
  - start crossover routes here
    - (space on sides and subset connect guaranteed)
  - recurse on left and right subtrees
- Essentially linear in number of switches

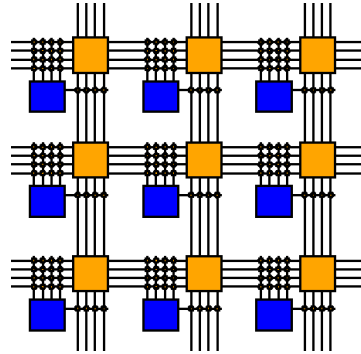
# Mesh

# Mesh



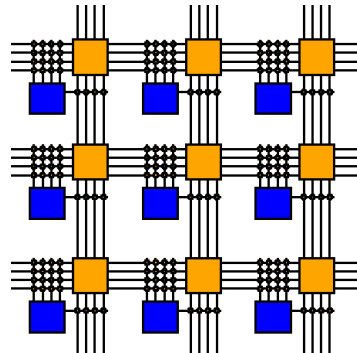
## Mesh Channels

- Lower Bound on  $w$ ?
- Bisection Bandwidth
  - goes as  $cN^p$
  - $\tilde{O}(N)$  channels in bisection
  - $w \geq cN^p / \tilde{O}(N) = cN^{p-0.5}$



## Straight-forward Switching Requirements

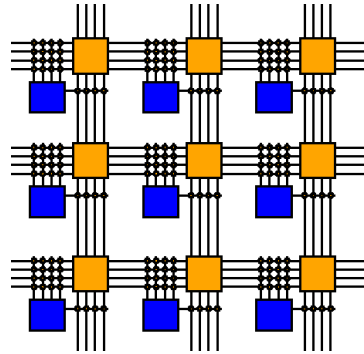
- Total Switches?
- Switching Delay?





## Switch Delay

- Switching Delay:  $2 \tilde{O}(N_{\text{subarray}})$ 
  - worst case:  $N_{\text{subarray}} = N$

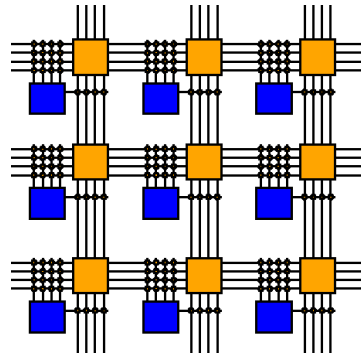


Caltech CS184a Fall2000 -- DeHon

17

## Total Switches

- Switches per switchbox:
  - $4 \cdot 3w \cdot w = 12w^2$
- Switches into network:
  - $(K+1)w$
- Switches per PE:
  - $12w^2 + (K+1)w$
  - $w^3 = cN^{p-0.5}$
  - Total  $\mu N^{2p-1}$
- Total Switches:  $N \cdot \text{Sw/PE} \mu N^{2p}$



Caltech CS184a Fall2000 -- DeHon

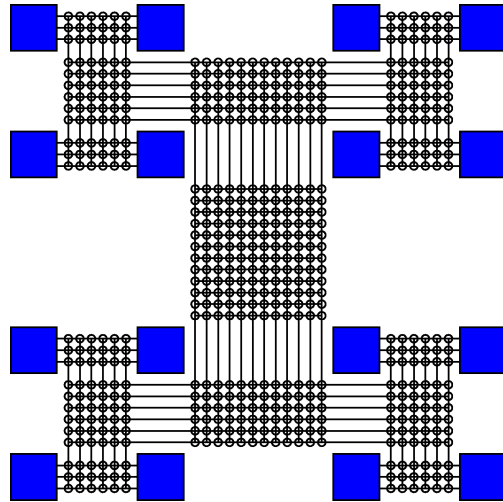
18

## Routability?

- Asking if you can route in a given channel width is:
  - NP-complete

## Meshes and Trees

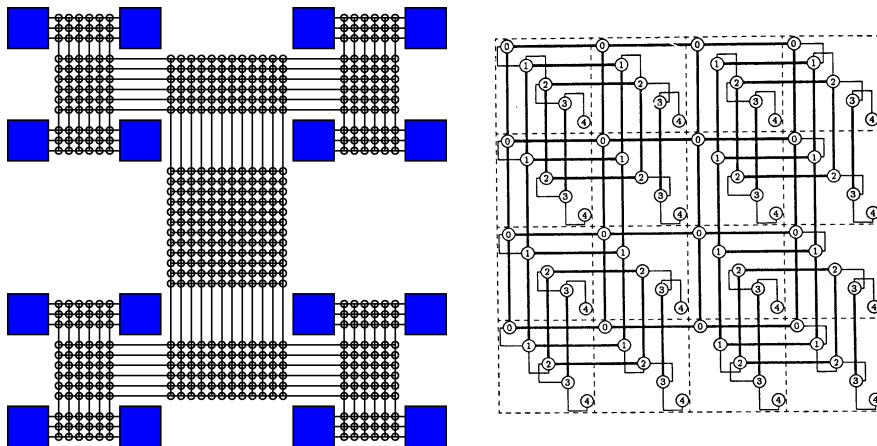
# Consider Full Population Tree



Caltech CS184a Fall2000 -- DeHon

21

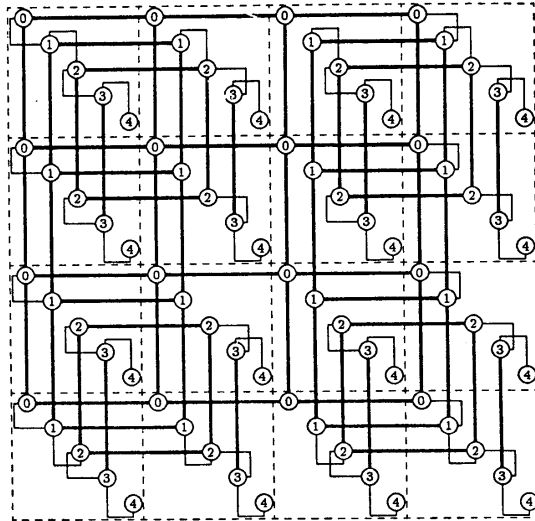
# Can Fold Up



Caltech CS184a Fall2000 -- DeHon

22

## Gives Uniform Channels



Works nicely  
 $p=0.5$

[Greenberg and  
 Leiserson,  
*Appl. Math Lett.*  
 v1n2p171, 1988]

Caltech CS184a Fall2000 -- DeHon

23

## How wide are channels?

- $W = [w(l) + w(l-1)]/ÖN$   
 $+ [w(l-2) + w(l-3)]/Ö(N/4)+...$
- $w_b(l) = c(2^l)^p$
- Share across  $\sim 2^{(l/2)}$
- $W = cN^{p-0.5}(1 + 2^{0.5}/2^p + 2^{2 \cdot 0.5}/2^{2p} + ...)$
- $W \mu N^{p-0.5}$  ( $p > 0.5$ )

Caltech CS184a Fall2000 -- DeHon

24

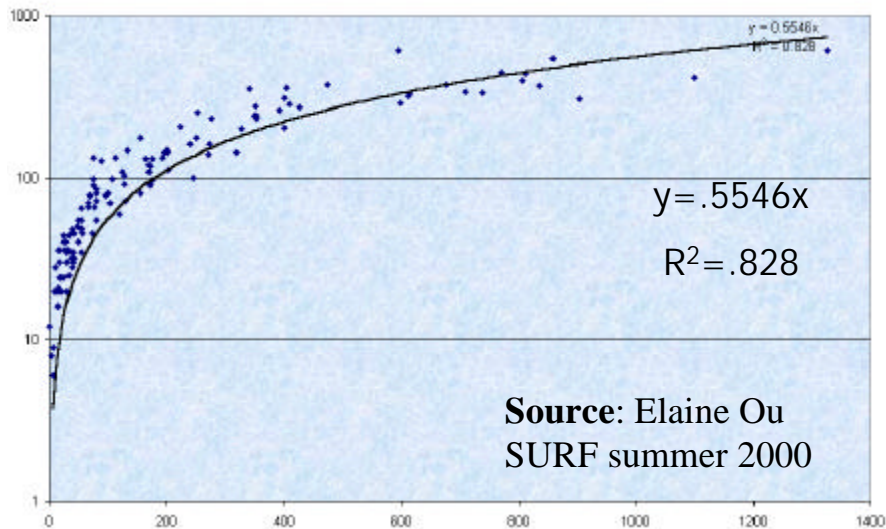
# Implications?

- On Mesh:
  - Upper bound on channel width
    - (assuming full population interconnect)
    - for something characterized by Rent's Rule  $c, p$
    - can use folded hierarchical routing
    - $w \propto N^{p-0.5}$
    - Same as lower bound, different constant
- On Hierarchical:
  - with this layout:
  - channels within constant factor of mesh

Caltech CS184a Fall2000 -- DeHon

25

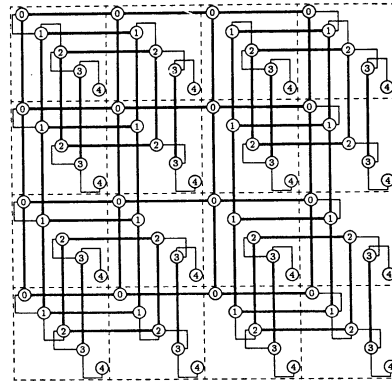
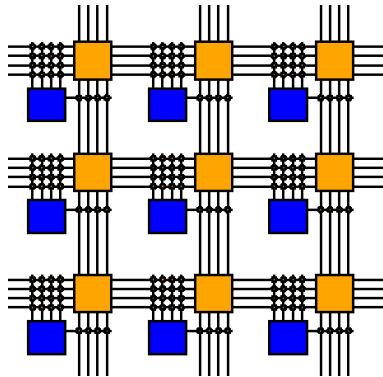
## Channel Width vs. $Cn^p$ (max Rent parameters)



Caltech CS184a Fall2000 -- DeHon

26

## What's Different?



Caltech CS184a Fall2000 -- DeHon

27

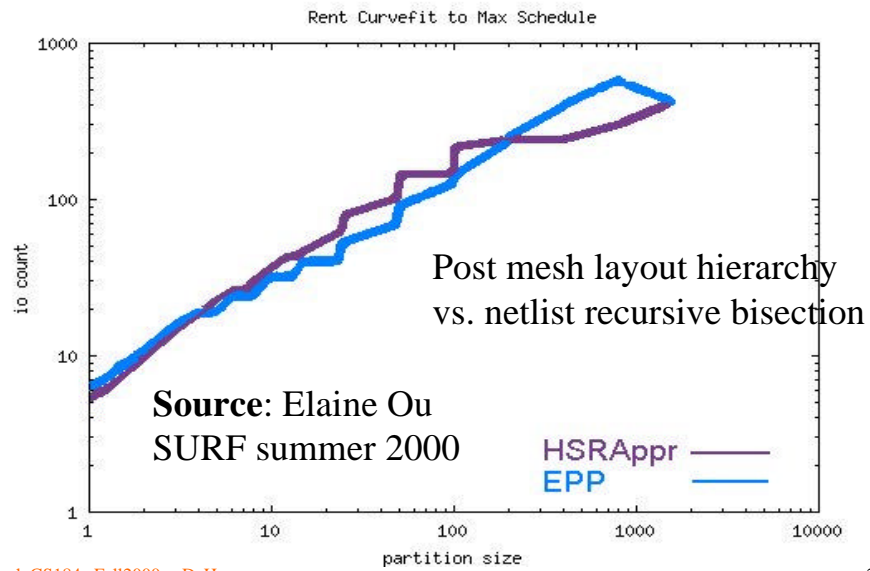
## What's Different?

- Logical and physical closeness
  - with shortcuts, tree has
- Switches in Path
  - $O(N)$  vs.  $\log N$ 
    - depends on how interpret switching nodes
- Mesh connect directly to any channel
- Hierarchical must to climb tree
  - part of how it manages to traverse only  $\log$  switches

Caltech CS184a Fall2000 -- DeHon

28

## Rent parameters from a large circuit



Caltech CS184a Fall2000 -- DeHon

29

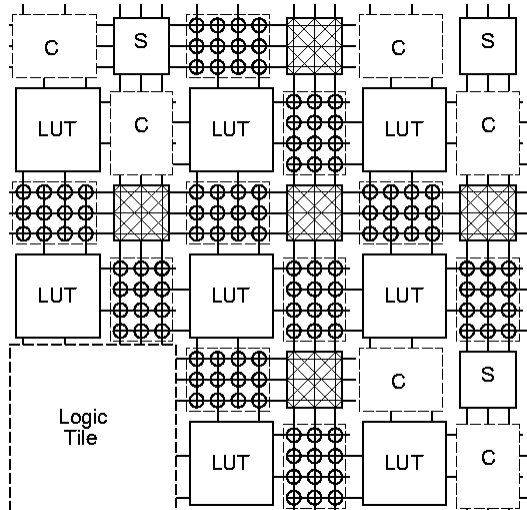
## Depopulation

Caltech CS184a Fall2000 -- DeHon

30

## Traditional Mesh Population

- Switchbox contains only a linear number of switches in channel width
  - $6w$  vs.
  - $12w^2$

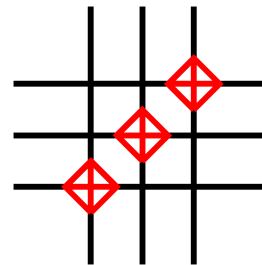


Caltech CS184a Fall2000 -- DeHon

31

## Diamond Switch

- Typical switchbox pattern:



- Many less switches, but cannot guarantee will be able to use all the wires
  - may need more wires than implied by Rent, since cannot use all wires
  - for mesh: this was already true...now more so

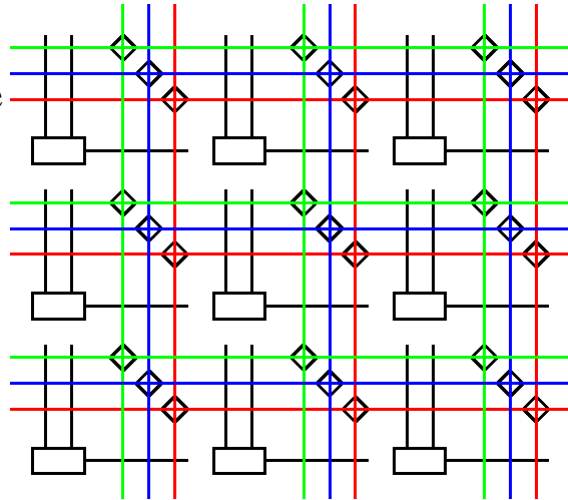
Caltech CS184a Fall2000 -- DeHon

32



## Domain Structure

- Once enter network (choose color) can only switch within domain

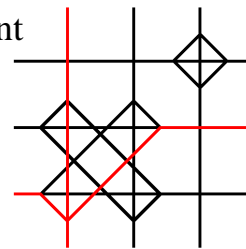


Caltech CS184a Fall2000 -- DeHon

33

## Universal SwitchBox

- Same number of switches as diamond
- Locally: can guarantee to satisfy any set of requests
  - request = direction through swbox
  - as long as meet channel capacities
  - and order on all channels irrelevant
  - can satisfy
- Not a global property
  - no guarantees between swboxes

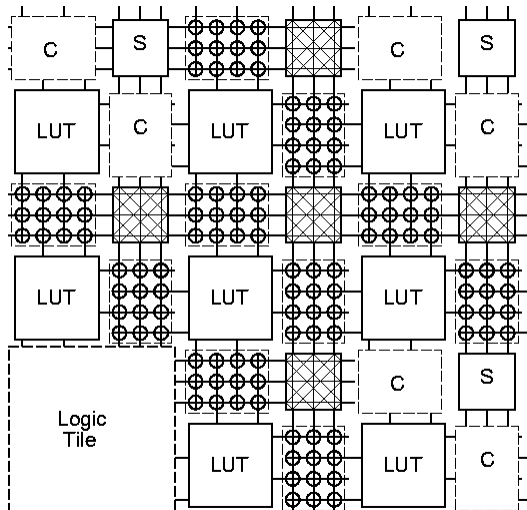


Caltech CS184a Fall2000 -- DeHon

34

## Inter-Switchbox Constraints

- Channels connect switchboxes
- For valid route, must satisfy all adjacent switchboxes



Caltech CS184a Fall2000 -- DeHon

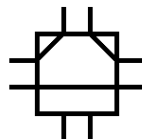
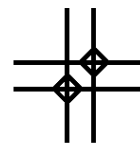
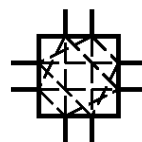
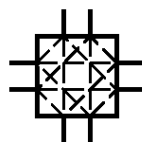
35

## Diamond vs. Universal?

- Universal routes strictly more configurations

Universal

Xilinx



can't route  
(or rotations)

Caltech CS184a Fall2000 -- DeHon

36

## Mapping Ratio?

- How bad is it?
- How much wider do channels have to be?
- Mapping Ratio:
  - detail channel width required / global ch width

## Mapping Ratio

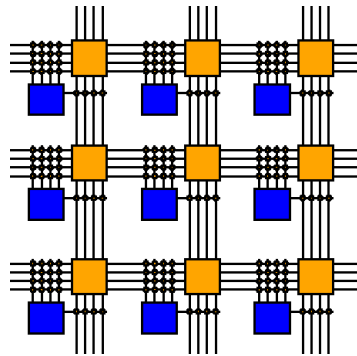
- Empirical:
  - Seems plausible, constant in practice
  - anecdotal/published data usually has mapping ratio  $< 1.5$
  - Elaine's data was detail
    - supports CMR model
- Theory/provable:
  - There is no Constant Mapping Ratio
  - can be arbitrarily large!

## Switching Requirements

- Linear Population Mesh
- Assuming a constant mapping ratio
- $S_w/sw_{box} = 6w$
- $sw/LUT = (K+6+1)w$
- $w\mu N^{p-0.5}$
- $SW/LUT\mu N^{p-0.5}$
- Total Switches  $W \mu N^{p+0.5} < N^{2p}$
- Switches grow slower than wires

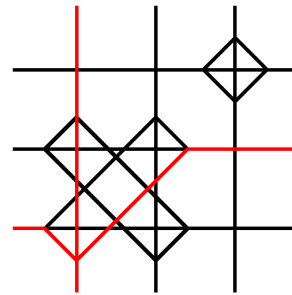
## Checking Constants: Full Population

- Wire pitch =  $8\lambda$
- switch area =  $2500 \lambda^2$
- wire area:  $(8w)^2$
- switch area:  $12 \sim 2500 w^2$
- effective wire pitch:
  - $174 \lambda$
  - $\sim 20$  times pitch



## Checking Constants

- Wire pitch =  $8\lambda$
- switch area =  $2500 \lambda^2$
- wire area:  $(8w)^2$
- switch area:  $6 \cdot 2500 w$
- crossover
  - $w=234 ?$
  - (practice smaller)



Caltech CS184a Fall2000 -- DeHon

41

## Practical

- Since wires aren't dominating
  - under this cost model
  - when both grow at same asymptote
- Can afford to not use some wires perfectly
  - to reduce switches
- Just showed:
  - would take 20x Mapping Ratio for linear population to take same area as full population

Caltech CS184a Fall2000 -- DeHon

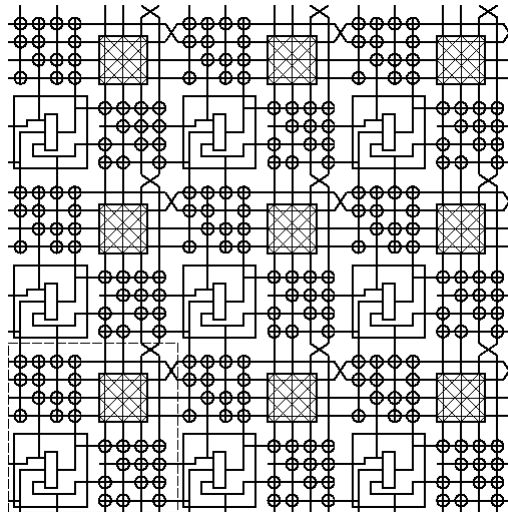
42

# Routability

- Domain Routing is NP-Complete
  - can reduce coloring problem to domain selection
  - (another reason routers are slow)

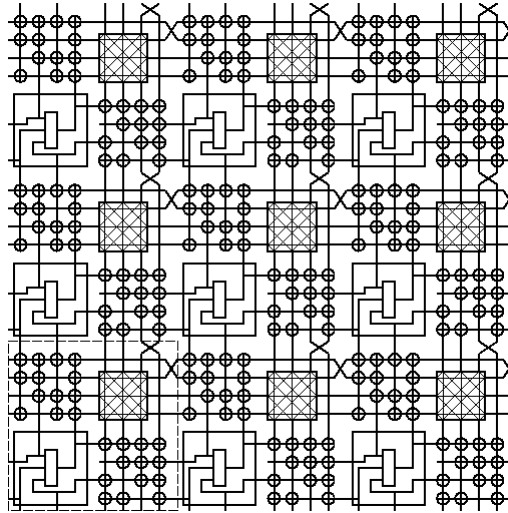
# Segmentation

- To improve speed (decrease delay)
- Allow wires to bypass switchboxes
- Maybe save switches?
- Certainly cost more wire tracks



# Segmentation

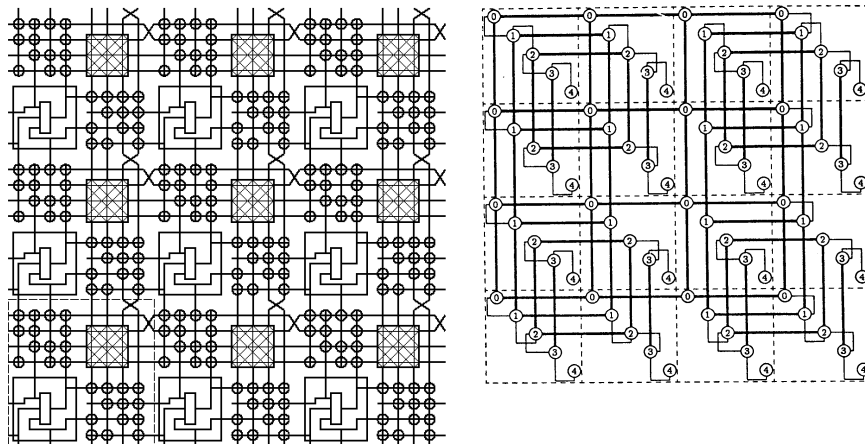
- Reduces switches on path
- May get fragmentation
- Another cause of unusable wires



Caltech CS184a Fall2000 -- DeHon

45

# Mesh with Hierarchy vs. Fold-and-Squash Tree?



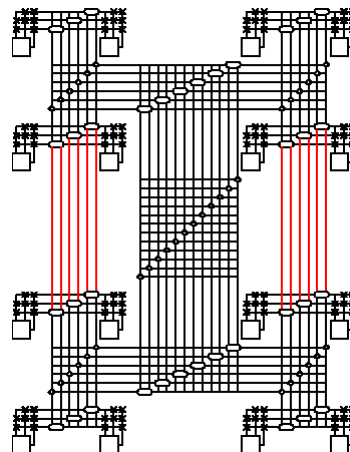
Caltech CS184a Fall2000 -- DeHon

46

# Depopulation in Tree

# Linear Population in Tree

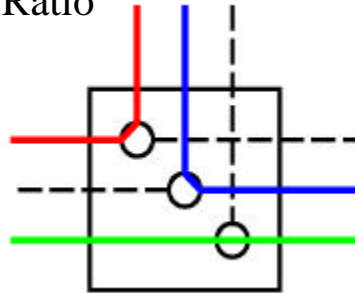
- Similar Strategy
- 3-way switch boxes
  - T: 3w (5w w/ short)
  - Pi: 5w (9w w/ short)





## Linear Population

- Will also have a Mapping Ratio
  - at least 1.5 on T stages



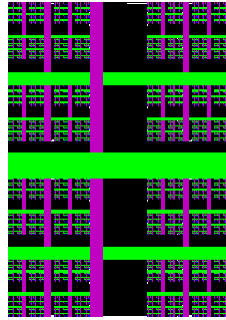
- But is it a constant mapping ratio?
  - Have not been able to prove
  - some evidence works in practice

## Switching Requirements Linear Population

- Key thing to note:
  - as go up the tree
  - half as many switchboxes
  - with (asymptotically)  $2^p$  more channels
  - $O(w)$  switches per channel
  - so  $2^p/2$  less total switches at each stage
  - ...simple geometric regression
- Total number of switches is linear in  $N$ 
  - compare everything else growing faster than  $N$

# Checking Constants

- 1024 PEs,  $p=0.67$   
 – shown to scale



Quadratic/perfect

Caltech CS184a Fall2000 -- DeHon C=5



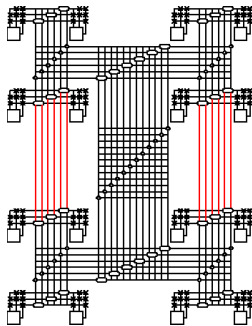
Linear  
C=8

**Again:**

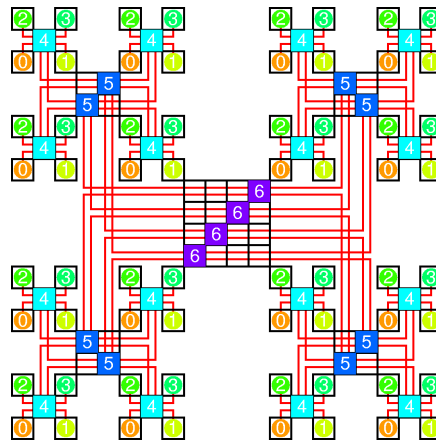
worth wasting  
some wires to  
reduce switch  
growth

51

# Fold and Squash Layout



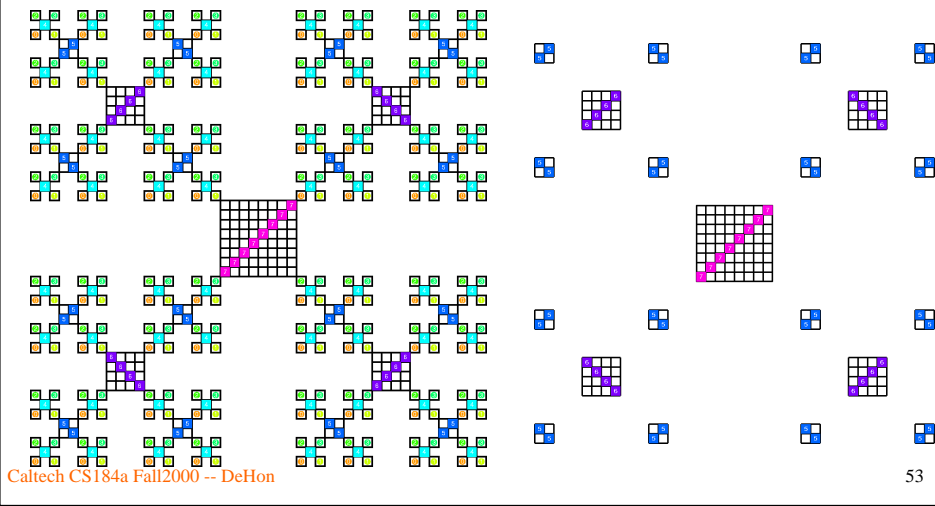
Caveat: may only work  
conveniently w/  $p=0.5$



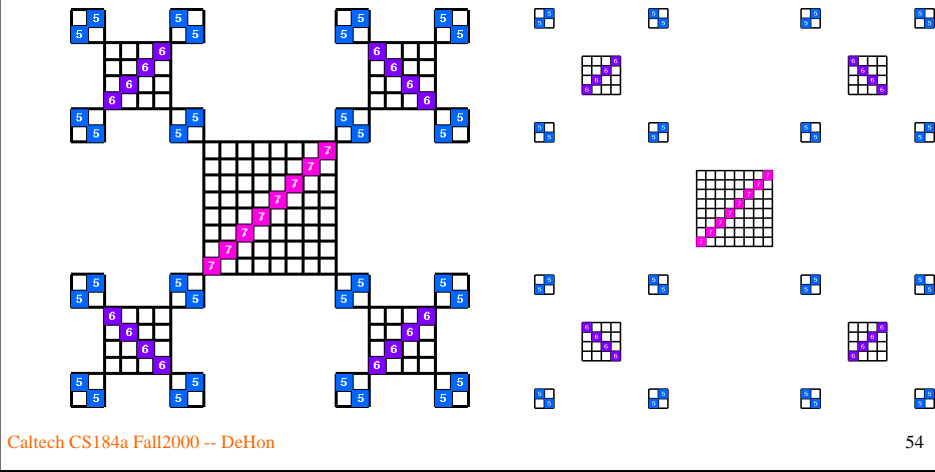
Caltech CS184a Fall2000 -- DeHon

52

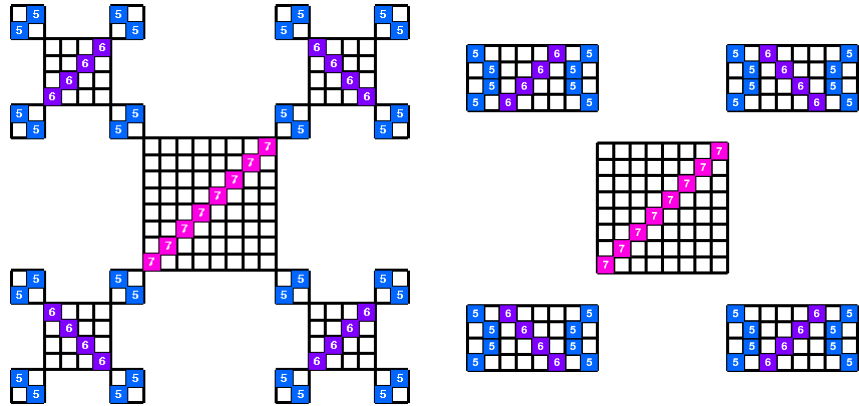
# Fold and Squash Layout



# Folding



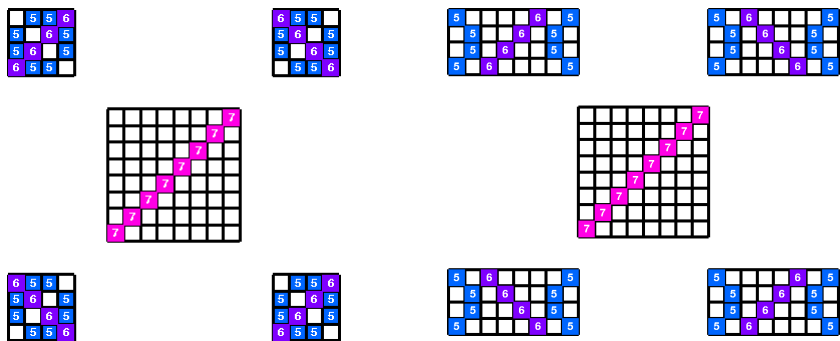
# Folding



Caltech CS184a Fall2000 -- DeHon

55

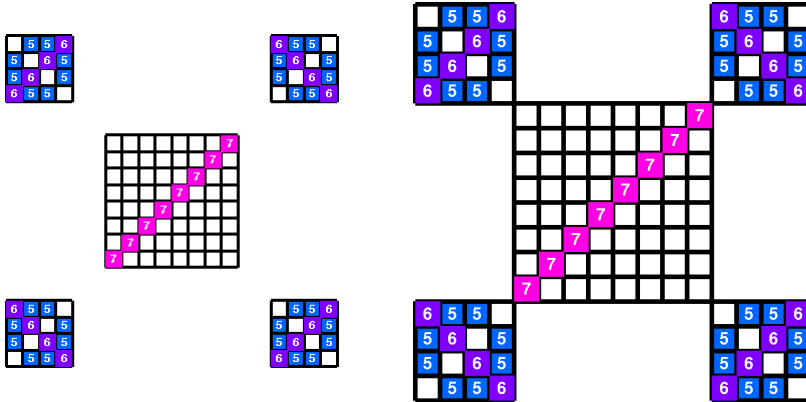
# Folding



Caltech CS184a Fall2000 -- DeHon

56

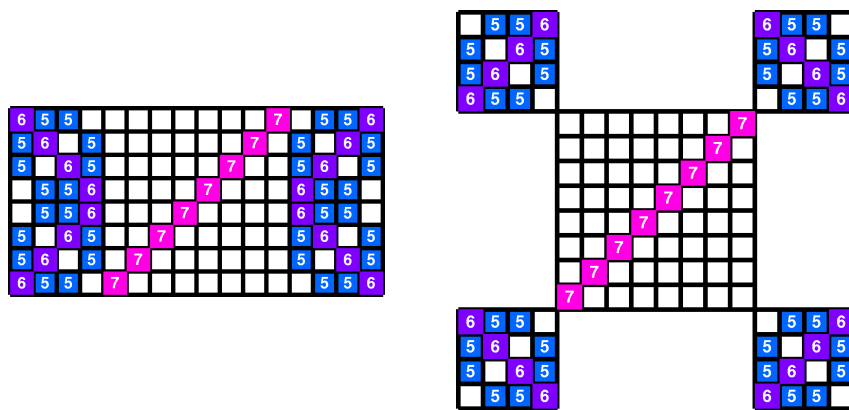
# Folding



Caltech CS184a Fall2000 -- DeHon

57

# Folding



Caltech CS184a Fall2000 -- DeHon

58

# Folding

6	5	5															7			5	5	6
5	6		5														7			5	6	5
5		6	5														7			5	6	5
	5	5	6														7			6	5	5
5	5	6															7			6	5	5
5	6	5															7			5	6	5
5	6		5														7			5	6	5
6	5	5															7			5	5	6

	5	5	6	6	5	5	7															
5		6	5	5	6	7	5															
5	6		5	5	7	6	5															
6	5	5		7	5	5	6															
6	5	5	7		5	5	6															
5	6	7	5	5		6	5															
5	7	6	5	5	6		5															
7	5	5	6	6	5	5																

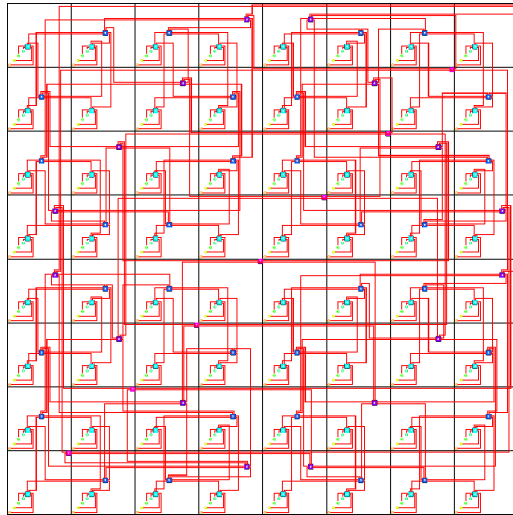
# Folding Invariants

- Lower folds leave both diagonals free
- Current level consumes one, leaving other free

	5	5	6	6	5	5	7															
5		6	5	5	6	7	5															
5	6		5	5	7	6	5															
6	5	5		7	5	5	6															
6	5	5	7		5	5	6															
5	6	7	5	5		6	5															
5	7	6	5	5	6		5															
7	5	5	6	6	5	5																

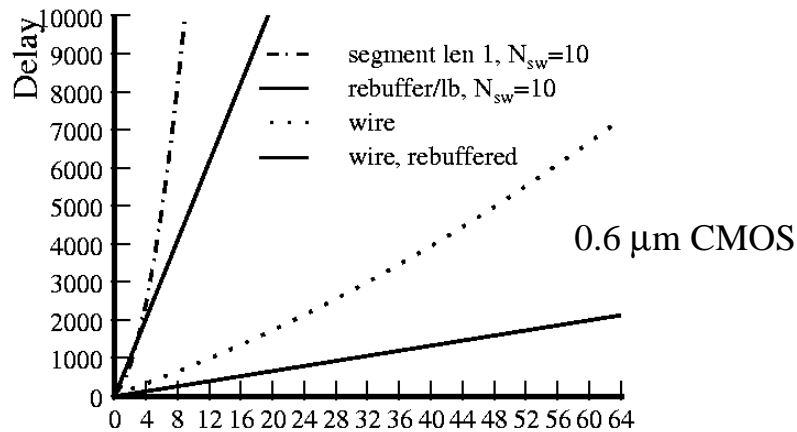
## Compact Folded Layout

- Can contain switches to constant area
- Wires still grow faster than linear
- Can use extra wire layers to accommodate wire growth
- (whereas switches not helped by additional wire layers)



## Switching and Delay

## Delay through Switching



<http://www.cs.berkeley.edu/~amd/CS294/notes/day14/day14.html>

Caltech CS184a Fall2000 -- DeHon

63

## Big Ideas [MSB Ideas]

- Cannot ignore switches
  - area or delay
- Switch population for guaranteed route
  - $O(N^{2p})$
  - like wires, but in CMOS switches larger
- Similarities of Hierarchical and Mesh
- Mesh w grow as  $N^{p-0.5}$

Caltech CS184a Fall2000 -- DeHon

64



# Big Ideas

## [MSB Ideas]

- Switchbox depopulation
  - save considerably on area (delay)
  - will waste wires
  - routing no longer guaranteed
  - routing becomes NP-complete
- Hierarchical/bypass routes
  - can reduce switching delay
  - costs more wires (fragmentation of wires)