California Institute of Technology
Department of Computer Science
Computer Architecture

CS184a, Fall 2000 # Assignment 6: Wiring Requirements Monday, October 30

Due: Monday, November 6, 10:30AM

In this assignment, I'd like you to develop a hands-on feel for the interconnect requirements for "typical" computations.

To continue the theme, we'll use the ALU and LUT logic decompositions you worked out last week as the designs we'll study. (Had I allowed you to use arrays of fixed-size PLAs, we could have looked at those as an alternative.)

For all exercises except the first, you should pick either your 4b-ALU or 4-LUT designs and use those. You should use the same media for all questions.

For all exercises except the last, you should work the problem separately for the three designs (control, datapath, and multiplier) and report all three results.

I'm hoping your designs are small enough (<100? maybe half that?) in terms of mapped units that these are not overly grungy tasks to think about–of course, I'm also hoping they are big enough this will be interesting. The logic in the datapaths might be big simply due to the width of the registers. If you choose to use the 4-LUT based design, you can reduce your datapaths to 6b in width. If you choose to use the 4b-ALUs, you can assume 12b datapath widths.

For areas, assume unit wire pitch and a switch area of 40 sq. units. Wires exist in separate planes above the switches. Where necessary, you may assume the interconnect dominates the non-interconnect area (that is logic block height or width is set only by the necessary interconnect pitches to which it connects).

For Delay: T_{lb} for logic block delay, T_{sw} for traversing a switch, T_w for crossing along a 100 units of distance on a wire. For simplicity, we're assuming linear wire delay and no additional charge for taps off of a line (for example, we'll be ignoring stub capacitance associated with switches which are on a line but we do not traverse along a path).

1. How many active outputs are there in each of your 3 designs? For the 4-LUT design, this is a single number. For the 4b-ALU design, I want to know both the number of 4b-busses, and the total number of wires (ok, it's just 4× the number of busses). This tells the number of signals we need to route simultaneously.

2. What is the IO to primitive logic block ratio for each of your three designs? This, too, tells us something (though crude) about the interconnect we need. If we keep the designs as a unit, we need at least that much wiring into a collection of that many gates.

   (*yes, the first two questions should be trivial for you to lookup from your last assignment.*)

3. Consider a crossbar implementation of each of your designs:

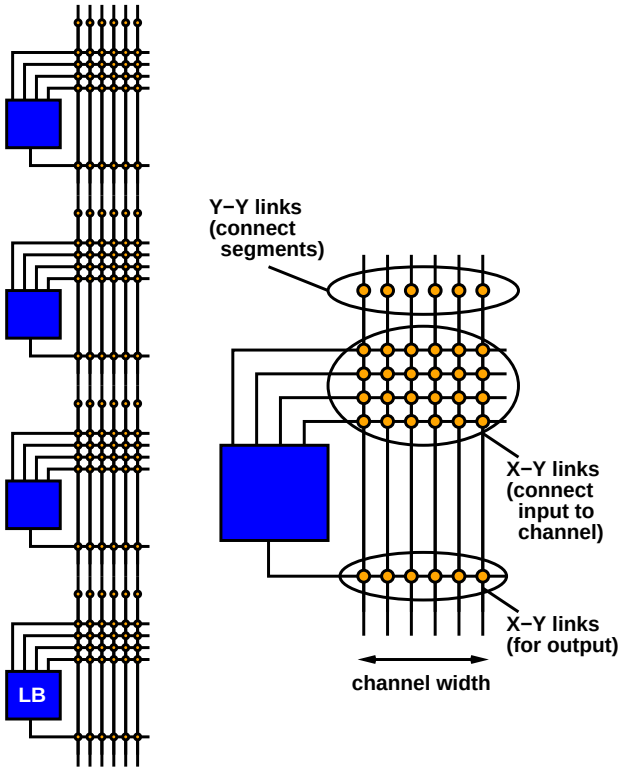
   (a) identify the size of the crossbar (inputs x outputs; for your own sake, justify the numbers)

   (b) what is the area for the crossbar?

   (c) what is the delay of a single link in the crossbar? (*i.e.* from one output to a connected input)

   (d) what is the critical path delay in your design?

4. Consider a 1D-segmented bus configuration:



   (a) layout your components in 1D to minimize the number of channels needed. (show your layout and routing in an appropriate, unambiguous manner; for your own sake, it will be useful to be able to easily see the span of wire segments.)

   (b) what is the channel width needed?

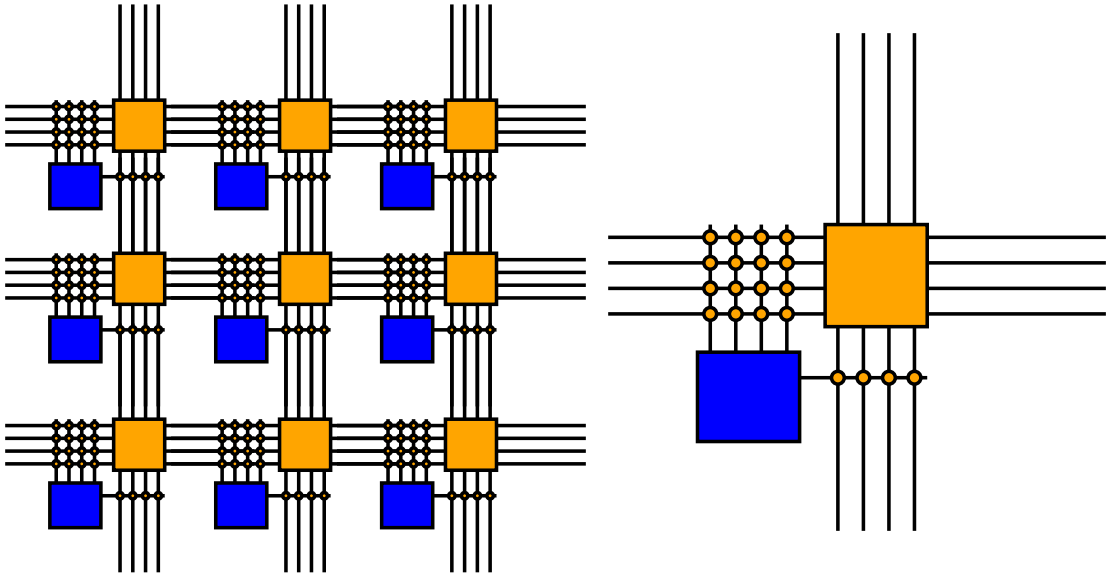
   (c) what is the area for the segmented bus interconnect?

   (d) what is the delay of the worst-case single link in use?

   (e) what is the critical path delay in your design?

   (f) what is the Rent schedule and Rent coefficients based on your 1D layout?

5. Consider a 2D-array configuration.
   (Assume the switchbox at the intersection of channels provides full connectivity to the adjacent channels. That is, it is made up of 4 $3w \times w$ crossbars; where w is the channel width. You may assume this block is switch dominated when calculating its area.)



   (a) layout your components in 2D.

   (b) route your design to minimize channel width. (I want a nice picture here which clearly shows each routed link and how routes share channels.)

   (c) what is the maximum channel width needed?

   (d) what is the area for the 2D interconnect?

   (e) what is the delay of the worst-case single link in use?

   (f) what is the critical path delay in your design?

   (g) how would you have designed your logic differently to reduce the delay for this kind of layout? (qualitative sketch)

6. Describe what happens when you put your three component designs together into the composite design for each of the three interconnect topologies examined here (single crossbar, 1D bus, 2D array). *Obviously, you've only been looking at pieces above, but these things would really want to coexist in one design. I don't want to ask you to work through the monolithic design in the details you worked through the pieces above. However, you should have enough of a feel for these things now, you can (more informally) sketch out the characteristics of the composite design.*