California Institute of Technology
Department of Computer Science
Computer Architecture

CS184a, Fall 2000 Background Questionnaire Monday, September 25

Please answer the following questions and return before leaving class today. This will **not** be used to affect your grade or enrollment in this class. I will use it to understand what students already know and how much variance there is among your backgrounds so I can better plan the course.

1. Name:
2. Email address:
3. Your status, year, and option (*e.g.* G1 CS):
4. What related courses have you taken? (if you've taken a non-caltech equivalent, please list what and where)
   - EE4 (digital logic)
   - EE5x (microprocessor/logic project lab)
   - CS20 (intro computer science)
   - CS181 (VLSI)
   - CS237 (compiler)
5. Other courses you are taking this semester (best estimate, fine):
6. Reduce the following to Minimum Sum-of-Products form:
   - $\overline{a} \cdot \overline{b} \cdot c + \overline{a} \cdot b \cdot \overline{c} + a \cdot b \cdot \overline{c} + a \cdot \overline{b} \cdot c$
   - $(a + b) \cdot (b + \overline{c})$
   - $(a + b) \cdot \left(\overline{b} + \overline{c}\right)$
   - $\overline{(b + c)} \cdot \left(\overline{a \cdot b}\right)$
7. How does the area of addition scale with n, the number of inputs to each of the operands? (delay?)

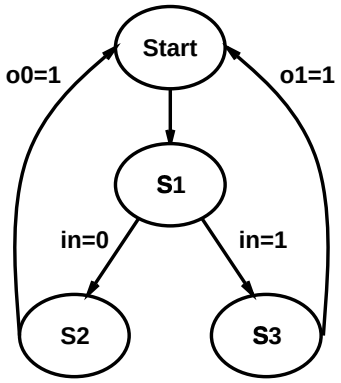
8. How does the area of an **arbitrary** n-input function scale with n? (delay? – explain your assumptions)

9. Express the following in Two's compliment (8b words):

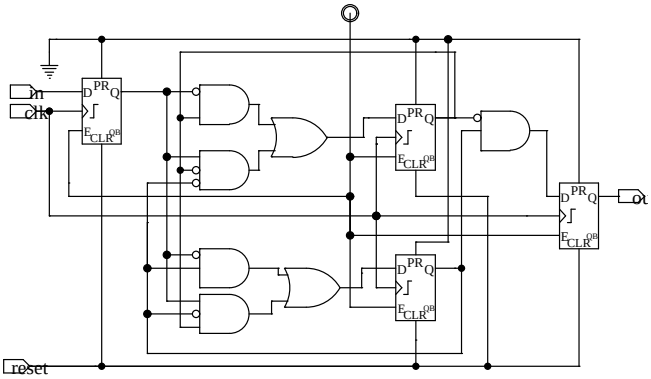
	← MSB							
decimal 10								
0								
decimal -1								
hexadecimal 23								
decimal -2								

10. Draw an ADDER bit-slice using only two-input NAND gates.

11. Write or draw logic to implement the following finite-state machine (one transition per clock, `in` is input, `o0`, `o1` outputs):



12. What is the function of this ciruit?



13. Identify the Latency and Throughput of above circuit (each gate = 1 time unit):

14. Describe a function which cannot be implemented in purely digital logic:

15. Briefly describe the relative benefits of each of the following (*i.e.* why/when would I want to use each over the alternatives?)

    - microprocessor
    - custom logic (ASIC)
    - PAL or FPGA