

California Institute of Technology  
Department of Computer Science  
Electronic Design Automation

CS137a, Winter 2002

Assignment #2

Monday, January 28

---

**Due:** Friday, February 8, 11:59pm.

**Resources** You are free to use any books, articles, notes, or papers as references. Provide citations in your writeup as appropriate.

**Collaboration** Please work independently on this assignment.

**Writeup** Writeup should be in an electronically readable format (HTML or PDF preferred, Word tolerated).

## Problems

1. As we have discussed, typical circuits have bisection widths smaller than  $n$  (for  $p > 0.5$ , Rent's Rule suggests a relationship  $IO = cN^p$ ). Sketch how we can use this property, along with one or more of the partitioning techniques we have been studying, to reduce the work required to find a satisfying assignment for a single-output logic cone; that is, an assignment of inputs that will make the output of the cone be true (note that once we have a way to do this, the extension to finding an assignment that makes the input false is trivial).
2. Formulate cost functions suitable for Simulated Annealing Placement for the following:
  - (a) Energy Minimization (similar model to last time, except that this time, we can control the capacitance associated with a switching node by reducing the wire-length which is attached to it)
  - (b) Point-to-point Distance Minimization
  - (c) Critical Path Delay Minimization
  - (d) Area Minimization (assuming cells live in an x-y grid, and inter-cell wiring does not run over cells)

For each comment on:

- How does optimizing the given cost function relate to the intended objective?
- How cheap/expensive is it to evaluate/update the cost function with each "move".

3. Answer questions 2 for Conjugate Gradient. [*At the moment, I don't know if the answer is exactly the same or different. I'm hoping to learn from the guest lecture. So the answer here could be trivial; in any case it will be a good thing for us to think about.*]
4. Sketch a constructive algorithm for 1D placement that uses replication to reduce wiring area. That is, use a model like our standard-cell row model from day 2:

$$A_{1D} = N_{cell} \times L_{cell} \times (W_{wire2wire} \times N_{wires} + W_{cell})$$

So, for example, replicating a cell to save one wire, would add one to  $N_{cell}$  and subtract one from  $N_{wires}$ . Try to find a solution with the flavor of the constructive placement algorithms we saw in class; do not use simulated annealing in this solution. Consider using one or more partitioning techniques and greedy refinement.