

# INTRO

The rise of technological advancement that we have experienced in the last 30 was in large part due to the rise in the number of transistors on a silicon wafer. The technological art that made this possible requires precise hardware manufacturing and efficient programming. Both the precision of hardware manufacturing and the efficiency of programming need to be maximized to get the most use out of a circuit on a silicon wafer.

The rise of nanotechnology is the latest wave of advancement in hardware manufacturing. We are now able to construct and program circuits on the molecular level. In the area of hardware manufacturing we have taken a great leap forward, which is in direction of smaller. While in efficiency of programming there has not been similar progress, which is in fact in the direction of larger. Here we try to develop an understanding possible architecture for a nanoscale circuit and do as well as suggest an efficient approach to partitioning such a circuit.

We will focus our discussion on efficient programming, yet our task will be two fold the architecture and partitioning. The architecture presented will be based on clusters of PLA. These PLA are nanoscale structures constructed using molecular level techniques. We will not focus on the hardware methods used to produce the PLAs. We will discuss how these PLAs will be arranged and placed in a circuit.

The main topic of the research paper will have to do with the efficient algorithms for partitioning. ...

## Architecture

The architecture most suitable for our logic circuit is that multi leaf tree. We will start out by having nano-wire mesh being constructed using molecular growth techniques. These meshes will be cut out into 60x60 nano-wire PLAs. This will provide our basic cross bar array. The ends of the wires will be stochastically doped to provide for the addressability of the nano-wires. The overlapping areas will be high or low in resistance depending if it is highly doped or pure. The same stochastic addressing will provide control and addressing at junctions of lithographic micro and nano wires. The nanowires will be layered out on top of the micro wires and depending on dopant concentration, will be able to conduct current through the junction. Hence we will have on and off switch that could function similarly to a transistor. This will require about  $2.2 \log(N)$  microscopic control wires for N number of nanowires. Hence a very small number of microscopic wires will control a large size nano-wire cross bar array.

We will efficiently partition these into clusters of 10x10 PLAs. The clusters will be portioned such that most of communication will be done within the cluster, which would be fastest. Such communication will be facilitated with nanowires connecting different PLAs within a cluster. We will also use stochastic addressing discussed above to control or address the individual "path" within a particular PLA. Thus we will employ the same techniques for control and addressing on both PLA and cluster level.

The final circuit will be a composition of a large number of scalable and programmable clusters of PLAs. These branch out in a tree and leaf formation. They will be interconnected by a micro scale bus system, the tree. And each leaf will be a cluster. The micro scale bus system will allow us to program and control the individual crossbars. At the same time the micro scale bus system will also allow for the transfer of information and communication between clusters. For this we will need to have a micro scale decoder so that we could access information most efficiently.

## References

André DeHon, [Stochastic Assembly of Sublithographic Nanoscale Interfaces](#) in IEEE Tr. Nanotechnology, September 2003

André DeHon, Nanowire-Based Sublithographic Programmable Logic Arrays in FPGA 2004